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13. ABSTRACT (Maximum 200 words)

We summarize our technical progress towards developing a thin-film edge emitter vacuum transistor capable of 1 GHz modulation. Design of the thin-film-edge emitter microwave vacuum transistors was completed this quarter. The first fabrication run of these devices is presently in progress. In addition, the design, assembly and characterization of two prototypes of high frequency probes that will allow on-wafer testing of the vacuum transistors was completed.

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Quarterly Technical Report

RF Vacuum Microelectronics

4/1/93 - 6/30/93

Sponsored by: Defense Advanced Research Projects Agency
Defense Sciences Office (DSO)
RF Vacuum Microelectronics
ARPA Order No. 8162
Program Code No. 1M10
Issued by DARPA/CMO under Contract #MDA972-91-0030

Contractor: Honeywell Sensor and System Development Center
10701 Lyndale Avenue South
Bloomington, Minnesota 55420

I. Executive Summary

Technical Approach: Our technical approach is to utilize thin film technology and surface micromachining techniques to demonstrate an edge emitter based vacuum triode. An array of vacuum transitors are connected in parallel to achieve microwave performance. The edge emitter triode approach offers several potential advantages to achieving high frequency device operation (compared to cone emitters or wedge emitters):

- Thin film processes for the films used in the triode process are well controlled and reproducible. Control of film thicknesses to within 5% for the emitter film thickness is easily attainable resulting in a well-controlled edge emitter.
- Device capacitance for the edge emitter is less than that achievable for cones or wedges resulting in potentially higher frequency operation.
- The fabrication process is a planar process, compatible with most silicon IC manufacturing.

Program Objective: **Demonstrate an edge emitter based microwave vacuum transistor with gain at 1 GHz continuously for 1 hour.**

Key Achievements (this reporting period)

- Completed the design of a thin-film-edge emitter microwave vacuum transistor.
- Completed the design, assembly and characterization of two prototypes of the vacuum feedthrough high frequency probes that will allow on wafer testing and characterization of microwave vacuum transitors.

II. Milestone Status

Milestone	Completion Date Planned	Actual	Comments
Task 1. Field Emitter Development			
Test Structure Design Complete	12/91	1/91	complete
Determine Workable Emitter Structure	3/92	3/92	complete
Demonstrate Emission Current of 10 μA/μm	11/92	11/92	complete
Deliver 10 Field Emitting Diodes	12/92	10/92	delivered
Task 2 Process Development			
High Resistivity Thin Film Resistor	4/92	9/92	complete
Complete Dielectric Studies	5/92	6/92	complete
Mechanical and Electrical FEM Analysis	5/92	8/92	complete
Task 3 Triode Development			
Triode Design Complete	4/92	5/92	complete
Demonstrate Reliable/Uniform Current Emission	7/92	10/92	complete
Demonstrate Modulated/Edge Emitter Triode	8/92	12/92	complete
Demonstrate 1 GHz Modulation of Triode	2/93	12/92	behind plan
Deliver 2 Triodes	3/93	8/93	behind plan
Task 4 Final Report (Baseline)	4/93	4/93	behind plan
Task 5 High Frequency Demo			
Design Microwave Vacuum Transitor	6/93	6/93	complete
Complete Process Development	6/93	6/93	complete
Complete High Frequency Probe Assembly	6/93	6/93	complete
Demonstate Vacuum Transistor with High Current	10/93	10/93	on plan
Demonstrate 1 GHz Modulation with Gain	10/93	10/93	on plan

III. Technical Progress

Efforts during this reporting period focused on the design of the microwave vacuum transistor and the fabrication of a high-vacuum microwave probe.

Task 1. Field Emitter Development

This task was completed at the end of the fourth quarter.

Task 2 Process Development

This task was completed at the end of the fourth quarter.

Task 3 Triode Development

This task was completed at the end of the sixth quarter with the demonstration of the vacuum transistor.

Task 4 High Frequency Triode Development

Our efforts in this quarter focused on:

- Microwave vacuum transistor design.
- Development of a vacuum feedthrough with high frequency probes for microwave measurements.

Microwave Vacuum Transistor Design

We designed a microwave vacuum transistors that can be probed on wafer through vacuum feedthroughs. The microwave vacuum transistor consists of an array of thin-film-edge emitter vacuum transistors that were demonstrated earlier in the program.. The vacuum transistor building blocks have emitter edge widths of 3 μm to 200 μm In order to reduce the device impedance and also to have sufficient gain, the microwave vacuum transistor is designed to have a nominal emitter current of 20 - 24 mA. Based on our earlier results of emission currents of 10 μa/μm of edge width, the microwave vacuum transistors have thin-film-edge emitters that are approximately 2400 μm long. The emitter cell width varies from 3 μm to 200 μm. These are grouped into 200 μm long segments, and twelve 200 μm long segments make a device. The cells and segments are interconnected by existing metal lines in the lower control electrode (LCE), upper control electrode (UCE), the emitter, the resistor and the anode/pad metallizations. Figures 1 and 2 show the side views of the device structure.

The microwave transistor has pad metallization that makes the device probable on wafer and can be tested at frequencies up to 2 GHz. The input (gate) and output (anode) pads are both surrounded by ground planes (emitter) on either side. The arrangement is very similar to devices that are designed to be probed by cascade microprobes. Figure 3 shows the top view of one of the devices. Details of device layout are given in the attached mask documentation.

The devices were designed based on the assumptions in Table 1 which is a summary of device results demonstrated earlier on in the program. Table 2 is a summary of the expected device performance. Figure 4 shows the device equivalent circuit used in designing the microwave vacuum transistor. For the 2400 μm wide device, we expect a current of 20-24 mA with a transconductance of 4 ms and a capacitance 408 fF. This should result in an f_τ of 158 GHz and a maximum available gain of 9.5 dB at 1 GHz. The microwave vacuum transistor design has been completed, and the fabrication masks have been purchased.

We started the first fabrication run and we have now completed 50% of the fabrication steps. The first fabrication run will be completed in mid-August and we shall begin DC tests immediately.

Microwave Vacuum Feedthrough Probes

We have designed new probes that will allow us to test microwave vacuum transistor at the wafer level. We have assembled two sets of probes.

The first set of probes used conventional vacuum feedthroughs in which the BNC connectors are grounded to the flange. Figure 5 is a diagram of the probes. The BNC connectors are fed by rigid coaxial cables to the device probes. The device probes are mounted on a 50Ω printed circuit board with a ground plane. The ground plane is connected to the emitter probe as well as the shields of the gate (input) and anode (output) coaxial cables. Figures 6 and 7 are measurements of insertion loss and feedthroughs of the probes. Figure 6 shows that the insertion loss is less than 5 dB at 1 GHz which is excellent, however the probe isolation is only about 20 dB as shown in Figure 7. This implies that any device that does not have at least -20 dB gain between the input and output could not be characterized. Our analysis is that the isolation between input and output is poor because the outer shield of the BNC connectors is grounded to the flange creating multiple grounds for the device under test and signal feedthrough between input and output. The low insertion loss indicates that input signals reach the probe tip without much degradation.

We ordered a new flange with two BNC connectors that have isolated shields. We constructed a similar probe to that described above. Figure 8 shows the insertion loss which is better than 5 dB at 1 GHz. The degradation above 1 GHz is due to the use of another connector between the BNC and the rigid coaxial cable. Figure 9 shows an isolation of better than 40 dB at 1 GHz showing an improvement of 20 dB over the first probe prototype. The results indicate that we should be able to feed signals to the device at 1 GHz without much signal degaradation and measure the output signal without much interference from the feedthrough signals.

The present probe assembly should allow us to test wafers in vacuum to a frequency of about 2 GHz. We are in the process of designing a third probe with isolated SMA connectors which should extend our testing capability to 8-10 GHz.

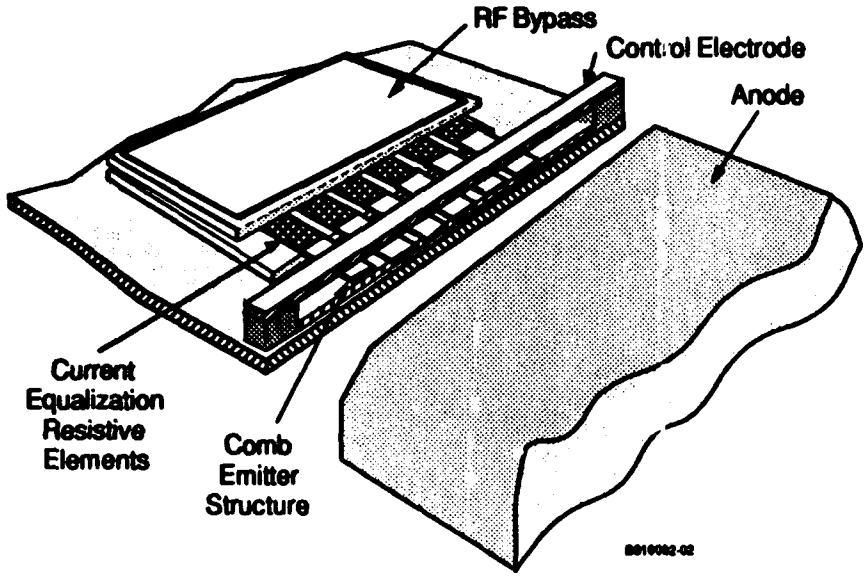
Plans for Next Reporting Period

- Complete fabrication of first VME processing run using the redesigned VME transistors described above.
- Complete DC characterization of VME devices fabricated in first run.
- Begin initial high frequency characterization of first run VME devices.
- Initiate second fabrication run of VME devices.

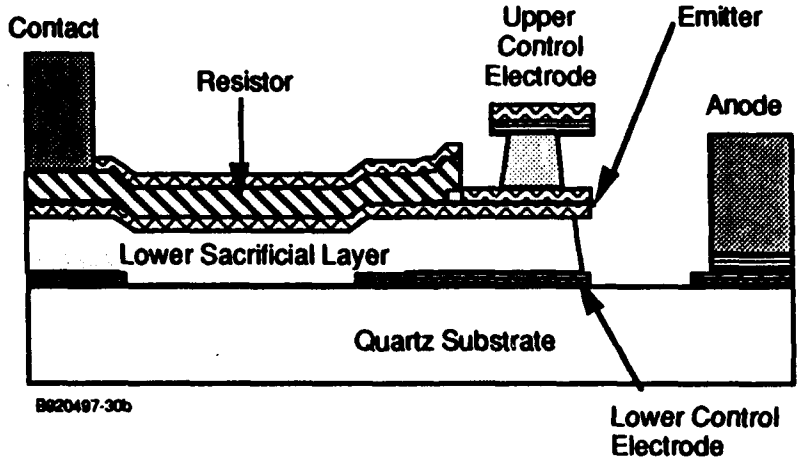
V. Programmatics

- A review of program status was given at the VME Tri Services Review in Washington, Dc at the end of June.
- Our paper entitled "Monolithic Lateral Thin-Film-Edge Emitter Vacuum Transistor" was accepted at the IVMC at Newport, Rhode Island Conference held mid-July 1993.
- Program progress was reviewed with Dr. Bob Parker and Dr. Henry Gray on May 4, 1993 at NRL.

Device Structure



Conceptual View of Vacuum Transistor



Side View of Vacuum Transistor

Figure 1

Device Structure II

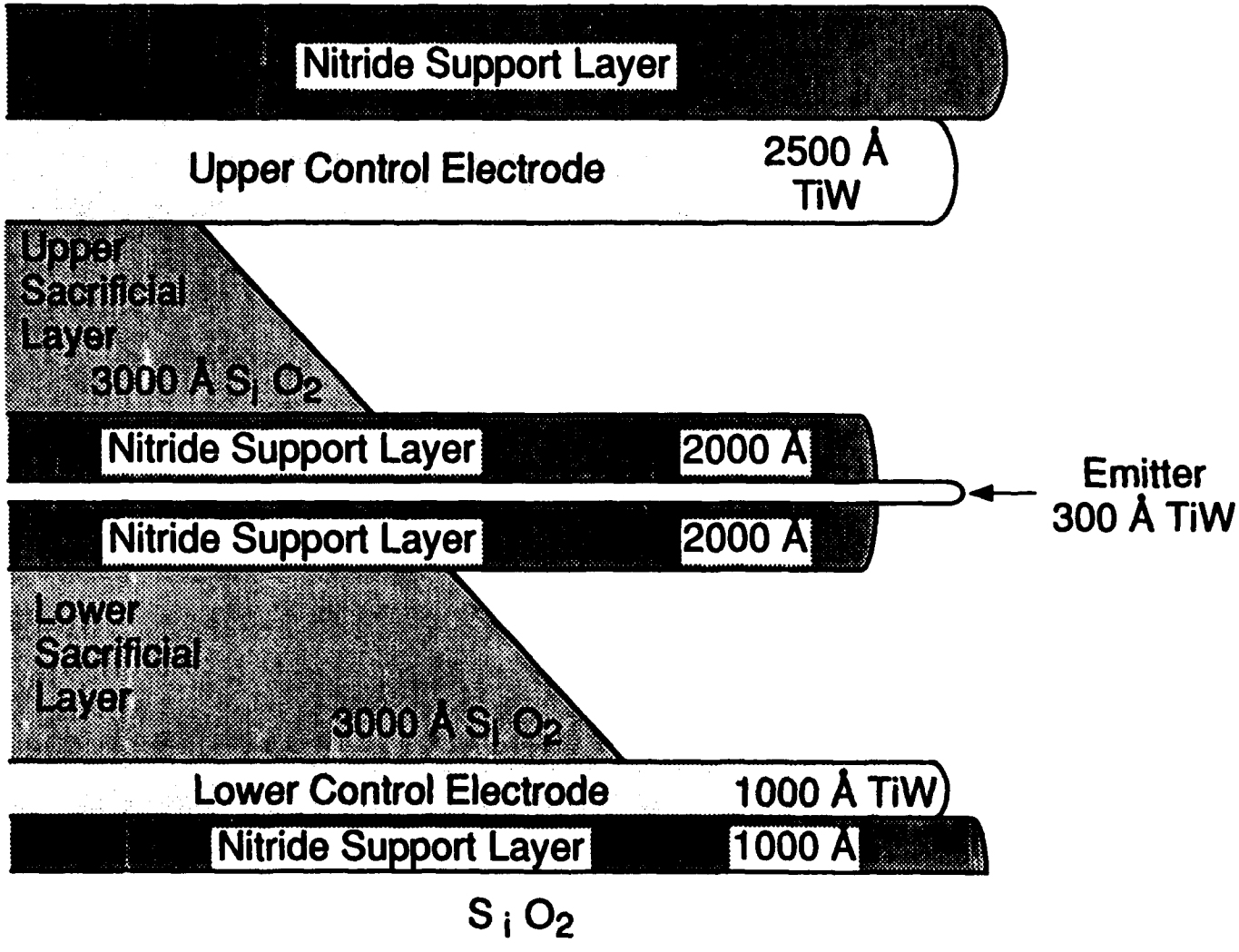


Figure 2

Microwave Vacuum Transistor Device Layout

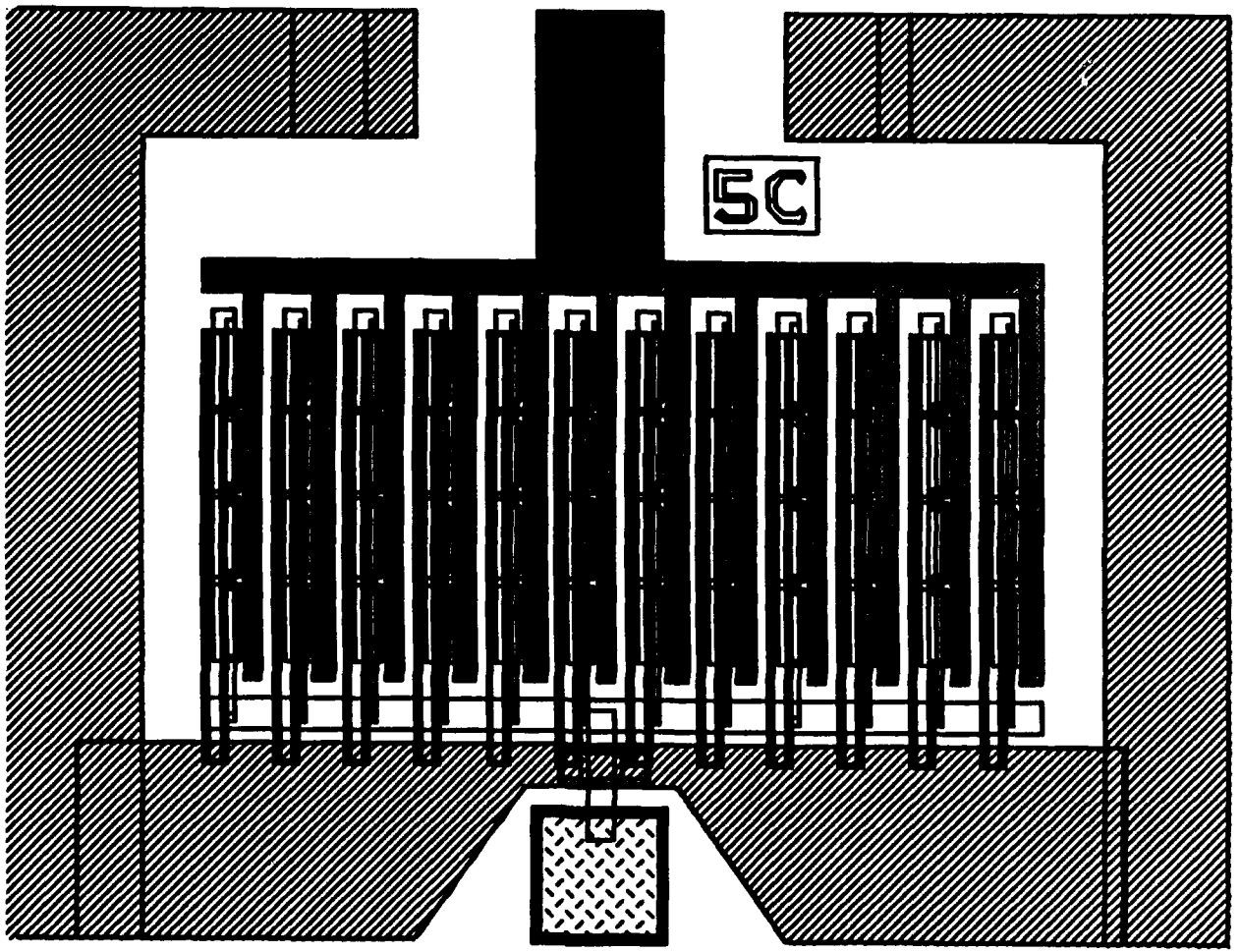


Figure 3

Summary of Device Results

Device Parameter	Measured Value
Device width (gate length)	4 μm
Turn-on voltage (0.1 μA)	50 V
Max current	50 μA
Current density	12.5 μA/μm
Extrinsic transconductance (including 1 MΩ resistor)	0.6 μS/μm
Intrinsic transconductance (excluding resistor)	1.5 μS/μm
Capacitance	0.3 fFarad/μm
f_τ (calculated)	1.06 GHz
Emission time (measured)	4 hours

TABLE 2

Microwave Vacuum Transistor Design Goal

Device Parameter	Device Value
Control electrode length	2 μm
Emitter current density	10 μA/μm
Transconductance	1.7 μS/μm
Input capacitance	0.17 fF/μm
Current gain cutoff frequency	1.58 GHz
Maximum available gain at 1 GHz	9.5 dB

Schematic Diagram Describing Field Emitter Triode Issues

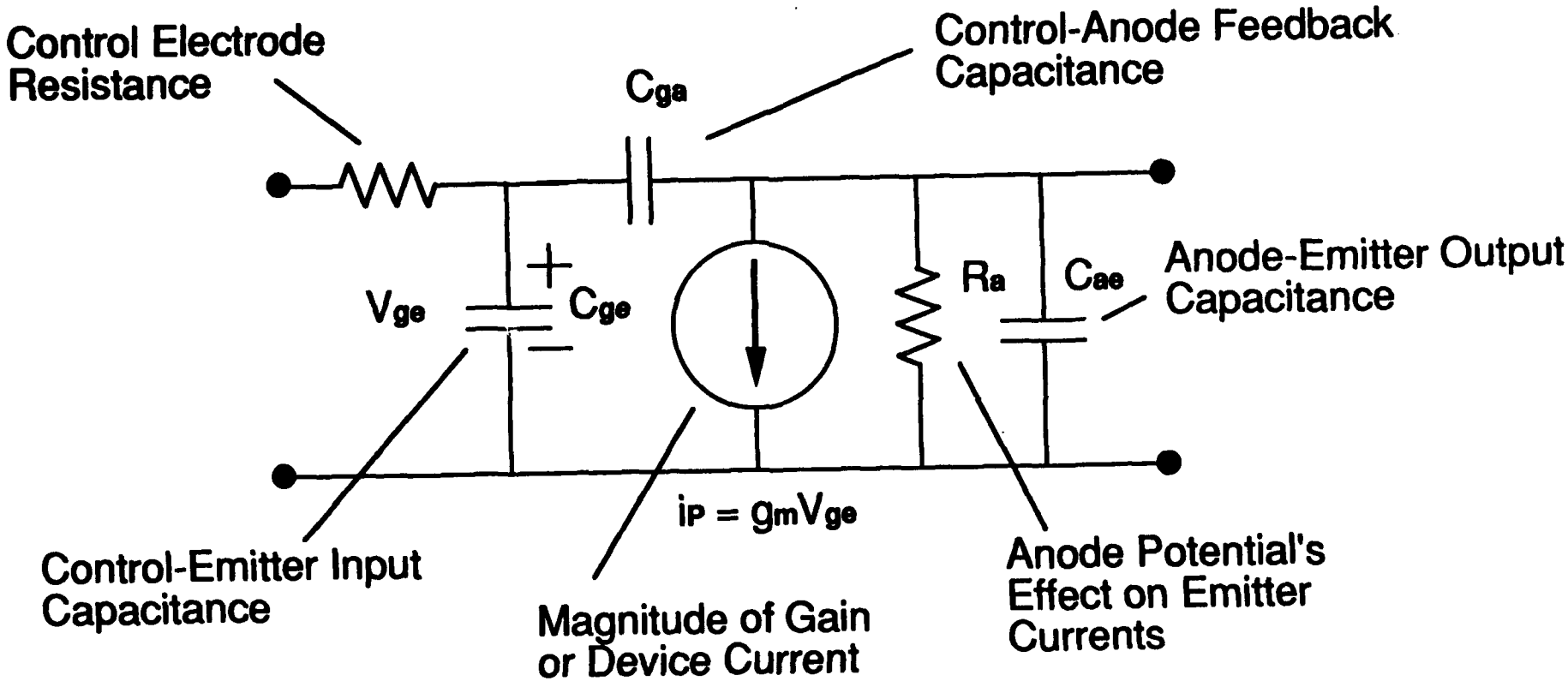


Figure 4

Vacuum Probe

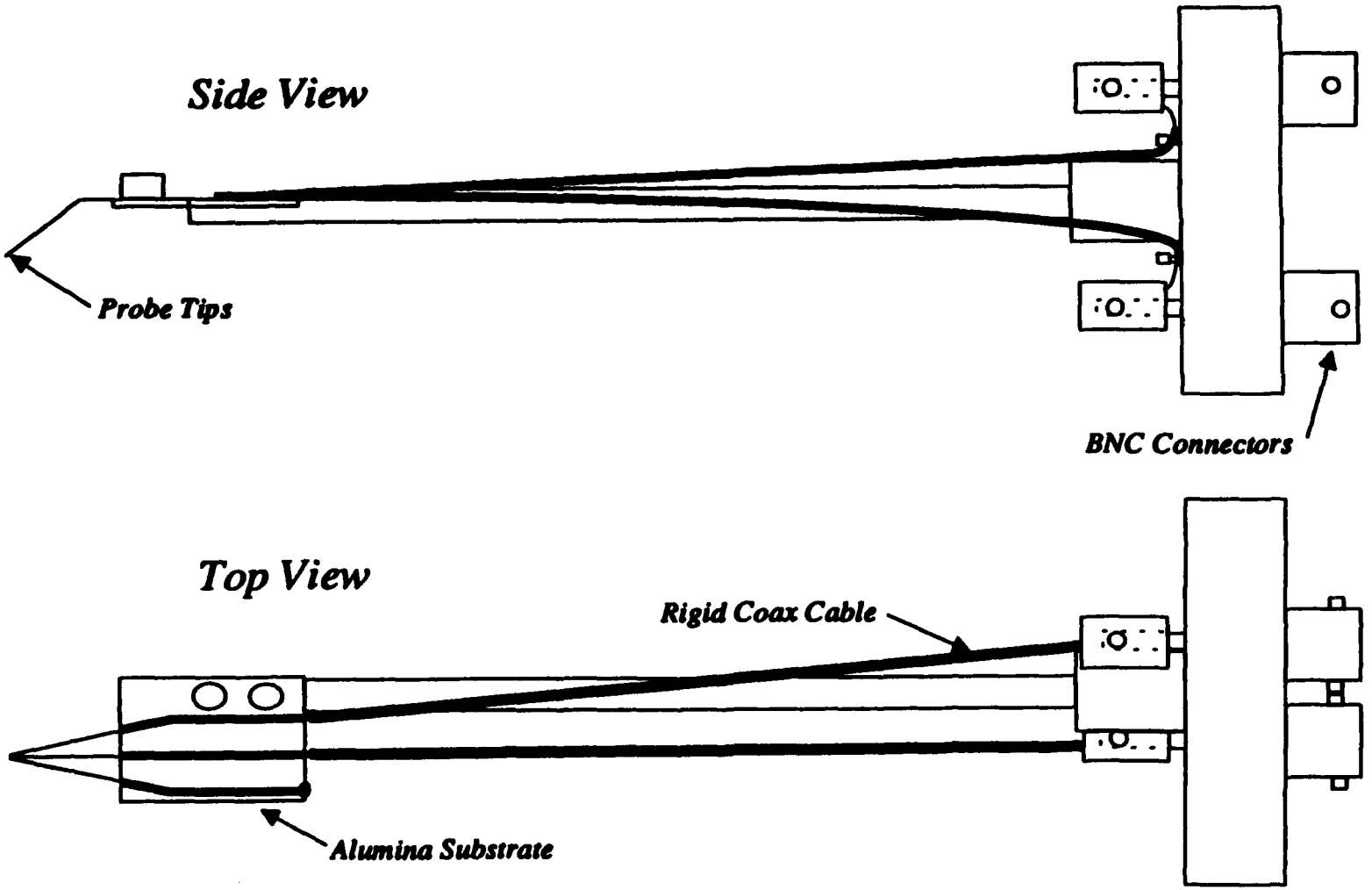


Figure 5

INSERTION LOSS - PROBE TIPS ON NIOMIL SQUARE GOLD PAD FOR THRU CONNECTION

PROBE DESIGN #1

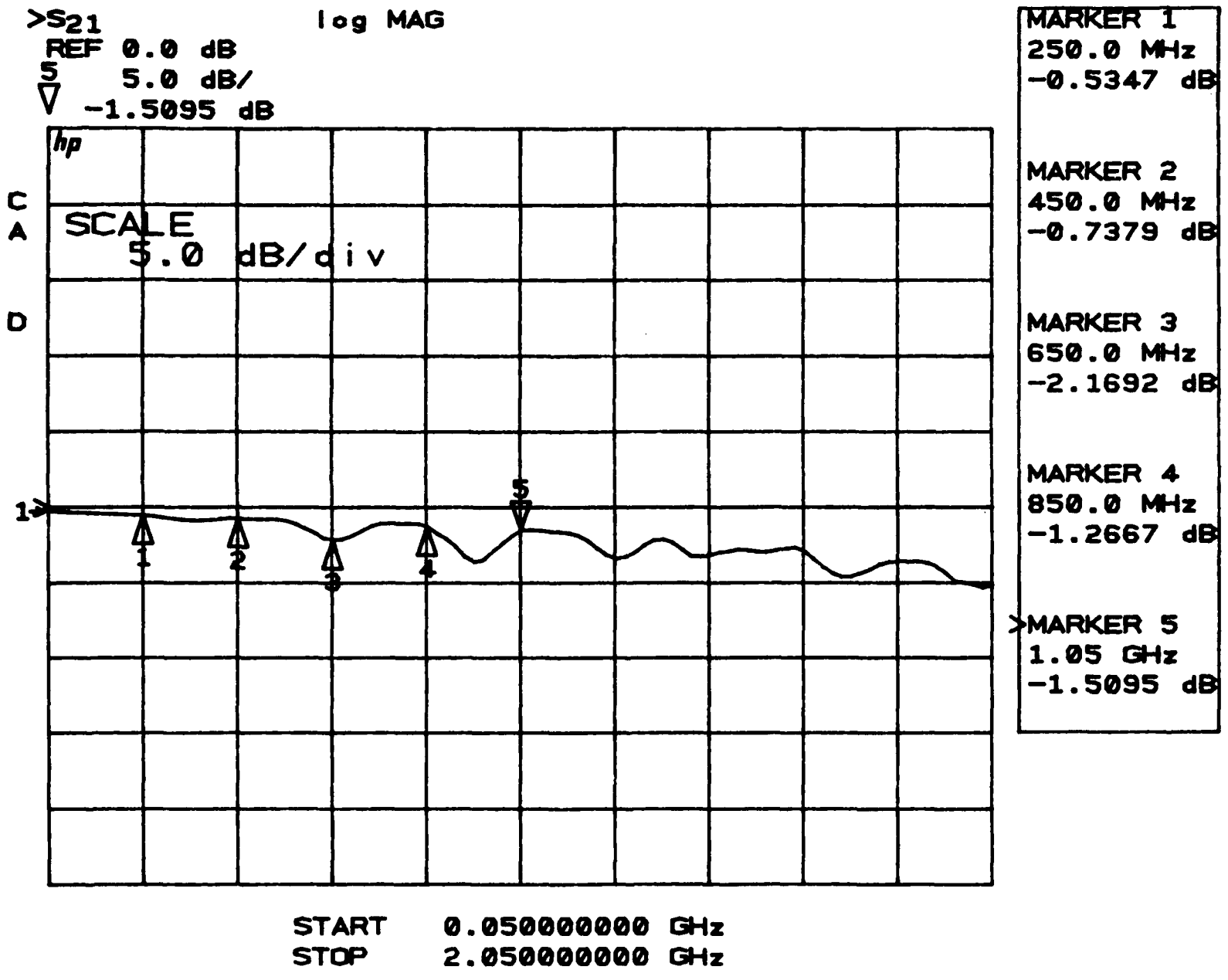


Figure 6

ISOLATION PROBE DESIGN #1

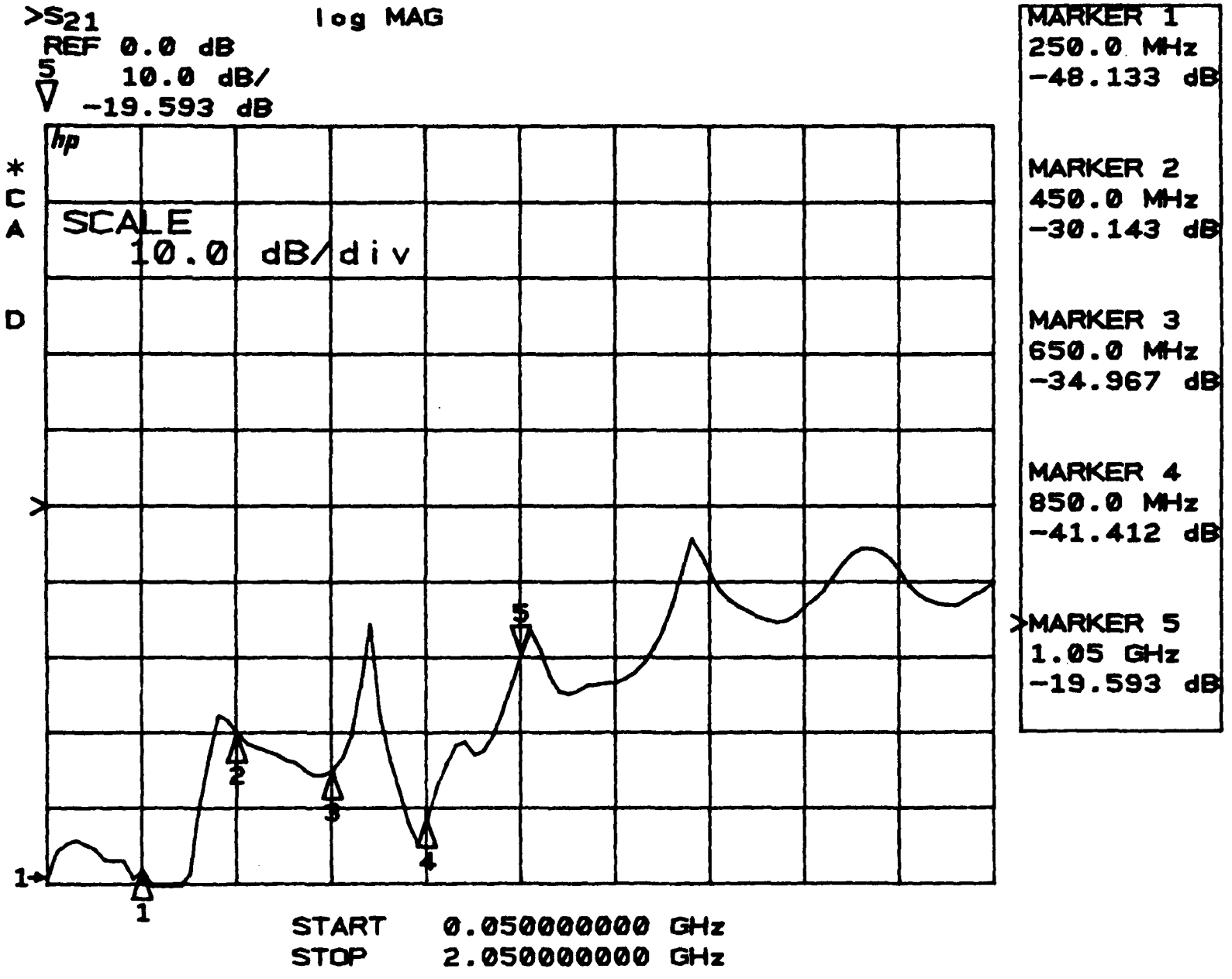


Figure 7

THRU CONNECTION - NO GROUND PROBE CONTACT

PROBE DESIGN #2

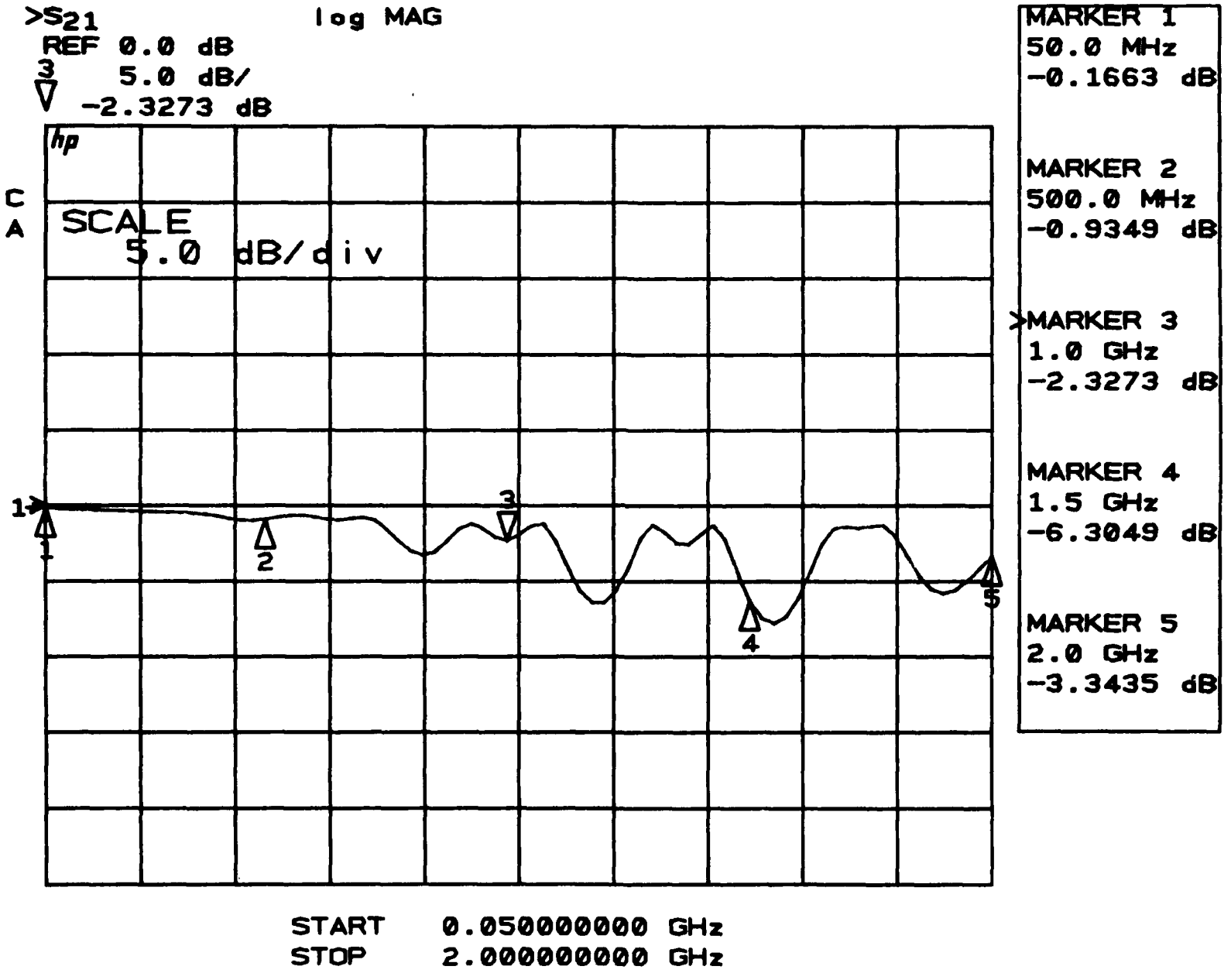


Figure 8

PROBE DESIGN #2

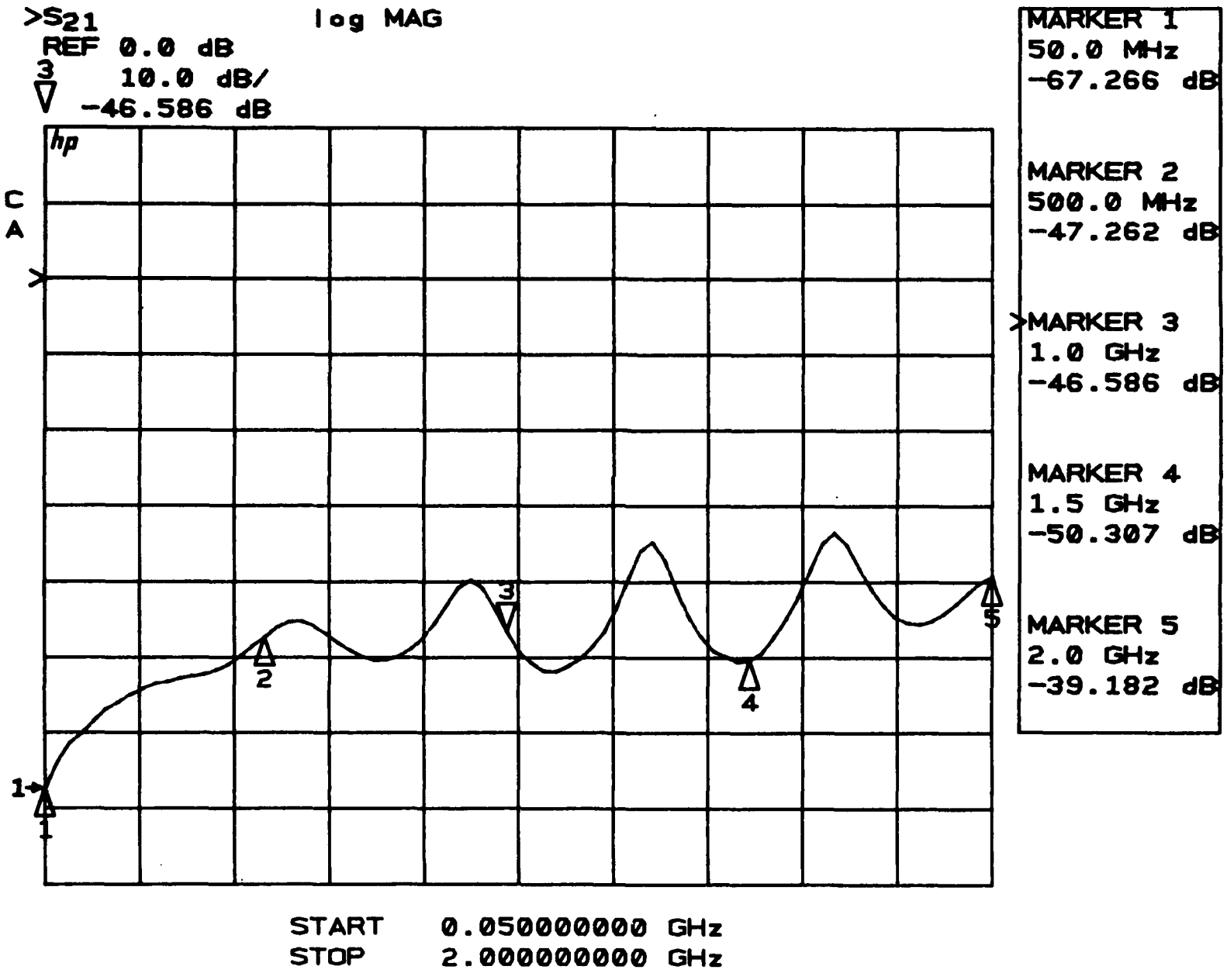


Figure 9

APPENDIX

VME Mask 5366 Layout Documentation

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June 25, 1993

1.0 Introduction

The primary issue in the development of vacuum microelectronic amplifiers is obtaining sufficient transconductance to overcome the effects of device input capacitances. Since the transconductance g_m is given by

$$g_m = \partial I/\partial V = I(2 + b/V)/V$$

and the collector current modulation is proportional to the magnitude of the DC current I while V is the control electrode bias voltage, high current densities with low input capacitances are required. The latter will be achieved only if emission is uniform. To obtain uniform emission the following factors are important:

- Uniform emitter geometries
- Homogeneous emitter surfaces
- Uniform control electrode geometries
- Bias control circuits to compensate for environmental factors

On a nanometer scale uniform emitter geometries are hard to obtain by fabrication alone and such properties will probably have to developed through improved treatments for the device after it is packaged. It appears that this is aided by operating the device while the emitter is at high temperatures. The thin film edge emitter is particularly advantageous in this regard in that it can easily be thermally isolated to an almost arbitrary degree to minimize heating power requirements. However, excessive thermal isolation may lead to destructive emitter temperatures. Uniform control electrode geometries and on-chip resistive bias control circuits are also readily implemented for some of the devices to be fabricated for this program.

The low stress materials required for device fabrication and adsorbed gases may also be a significant source of ions which will be released when the anode temperature increases during device operation. While they may be partially removed by heating the entire structure to high temperatures their impact on the emitter can lead to its destruction.

2.0 Reticle Description

The field emission triode arrays and a few test triodes devices in the 5366 mask set are described in Tables 2-1 and 2-2. Figure 2-1 has a cross section of one of the cells in the FET array. The triode name, e.g. 50, is the width of the smallest emitter cell in the triode in microns. The meaning of the letter suffix is summarized in Table 2-3. The location of the individual triodes in Table 2-2 is described by row and column from the

bottom and left side of the reticle in Figure 2-2. Row 0 describes the position of the test triodes which are located just above the alignment for record marks on the right of the in-process test devices. Most of the triode arrays are approximately 2400 μm wide and should have sufficient current capability for lower frequency microwave operation, i.e., with 10 μA/μm the total current should be 24 mA.

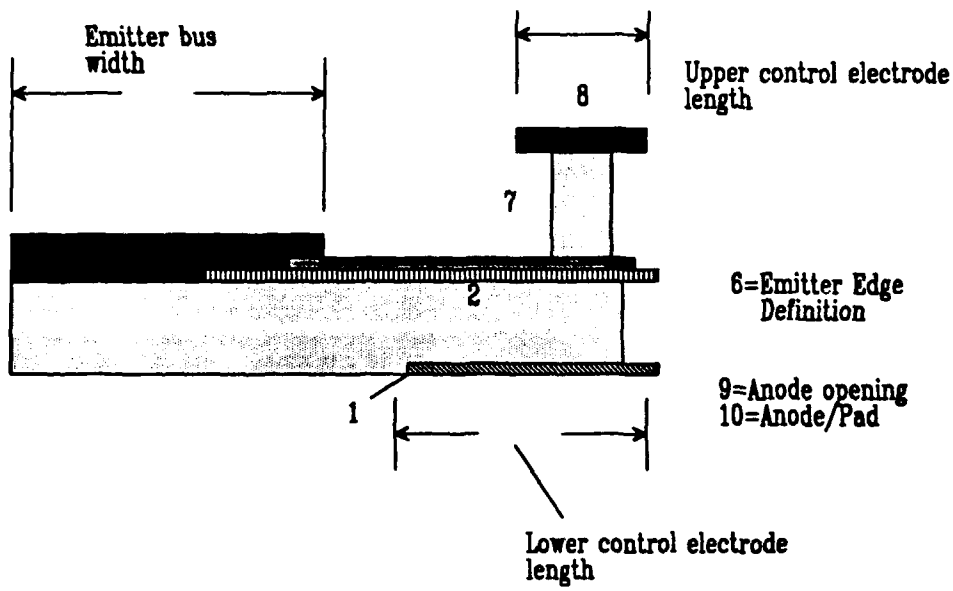

Figure 2-1 Cross section of a typical field emission triode emitter without series resistors showing the structure used

The layout of five of the different triode arrays is described in Figures 2-3 through 2-7 for devices using 50 micron width emitters. The total width of each emitter cell is approximately 200 microns wide but this is divided in different ways as described in the tables.

Table 2-1
Listing of Field Emitter Triodes in the 5366 Mask Set

Triode name	Symbol used in reticle	Upper control length (μm)	Lower control length (μm)	Emitter cell width (μm)	Emitter bus width level 2 (μm)	Number of Devices
51	51	5	17	3 x 6 x 12	12	6
51A	51A	5	3	3 x 6 x 12	12	6
50	5	3	17	50 x 4 x 12	12	3
100	1	3	17	100 x 2 x 12	12	3
200	2	3	17	200 x 1 x 12	12	3
50A	5A	4	3	50 x 4 x 12	12	5
100A	1A	4	3	100 x 2 x 12	12	6
200A	2A	4	3	200 x 1 x 12	12	5
50B	5A	3	3	50 x 4 x 12	12	6
100B	1B	3	3	100 x 2 x 12	12	6
200B	2B	3	3	200 x 1 x 12	12	6
50C	5C	5	17	50 x 4 x 12	12	6
100C	1C	5	17	100 x 4 x 12	12	6
200C	2C	5	17	200 x 1 x 12	12	6
50D	5D	4	3	50 x 4 x 12 w/res	12	3
100D	1D	4	3	100 x 2 x 12 w/res	12	3
200D	2D	4	3	200 x 1 x 12 w/res	12	3
50E	5E	3	17	50 x 4 x 9 w/series res	10	3
SPARSE	S	3	17	50 x 4 x 6	12	1
TR1	1	20	21	5 x 13 w/res	NA	1
TR17	17	3	21	5 x 4 w/res	NA	1
TR19	19	3	21	5 x 3 w/res	NA	1

Table 2-2
Field Emission Triodes by Row and Column Location

Row	Column(s)	Triode	Upper/lower control electrode lengths (μm)	Total emitter width (μm)
0 (Near test devices)	10	1	20/21	65
0 (Near test devices)	11	17	3/21	20
0 (Near test devices)	11	19	3/21	15
1	1-6	51	5/17	360
1	7-12	51A	5/3	360
2	1-3	200A	4/3	2400
2	4-6	50E	3/17	1800
2	7-12	200C	5/17	2400
3	1-3	200	3/17	2400
3	4-6	200D	4/3	2400
3	7-12	200B	3/3	2400
4	1-6	50C	5/17	2400
4	7-12	100C	5/17	2400
5	1-6	50B	3/3	2400
5	7-12	100B	3/3	2400
6	1-5	50A	4/3	2400
6	6	SPARSE	3/17	1200
6	7-12	100A	4/3	2400
7	1-3	50	3/17	2400
7	4-6	50D	4/3	2400
7	7-9	100	3/17	2400
7	10-12	100D	4/3	2400

Table 2-3
Alphabetic Suffix Used to Describe Control Electrode Lengths Except for Device 51 with a 5 μm Upper Control Electrode

Suffix	Upper Control Electrode Length (μm)	Lower Control Electrode Length (μm)
None	3	17
A	4	3
B	3	3
C	5	17
D	4	3
E	3	17

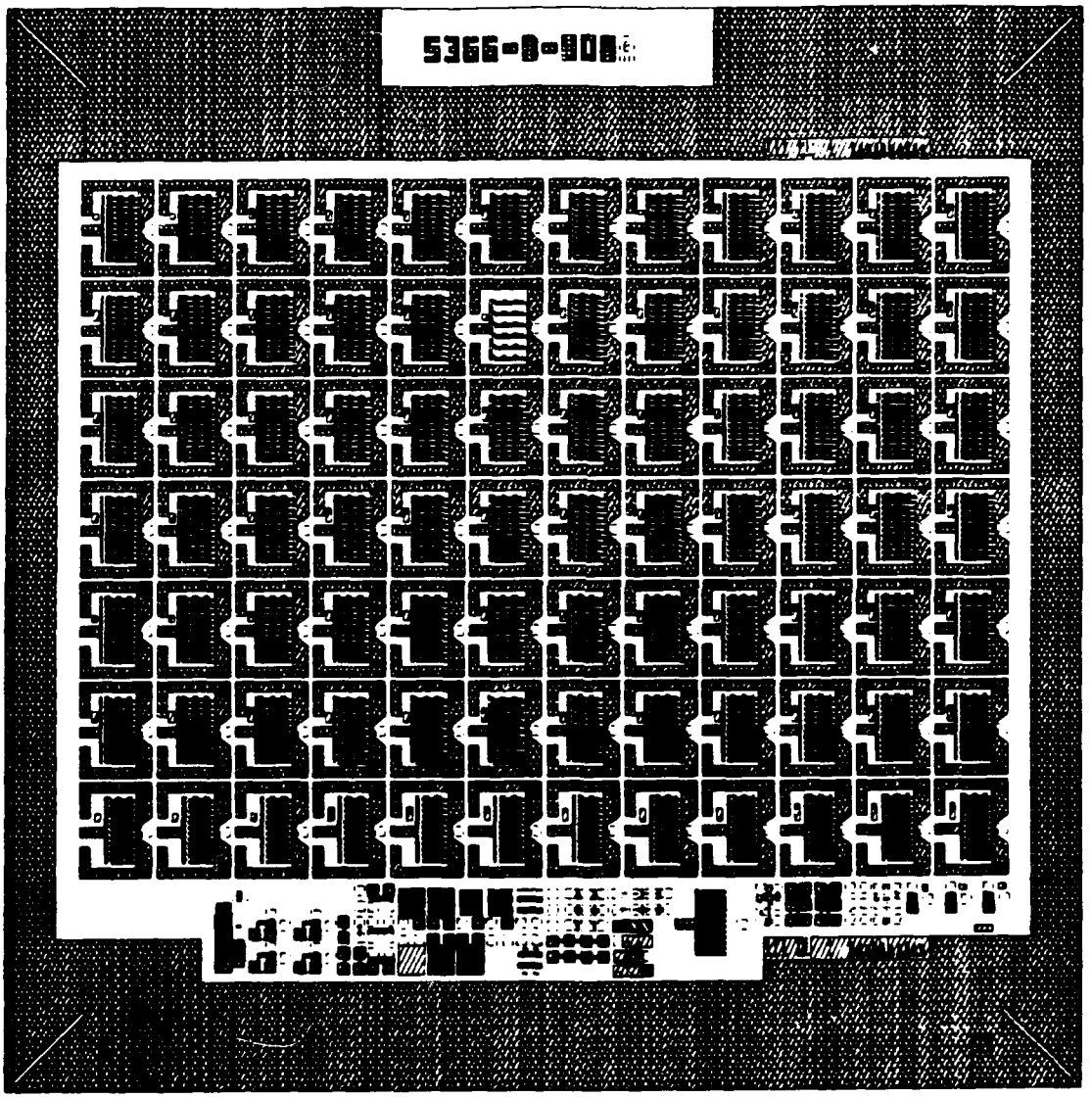

Figure 2-2 Reticle layout showing the position of the triode arrays and test structures

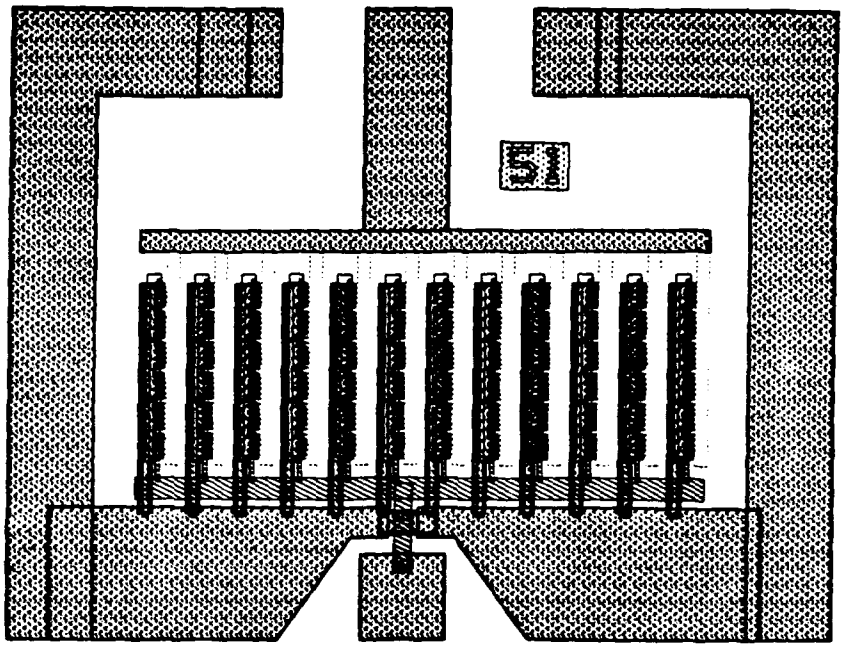

Figure 2-3 Triode 51 with 12 cells having (18) 5-micron wide emitters divided into 6 groups in each cell

Figure 2-4 Triode 50 divided into 12 cells that have four 50 μm wide emitters

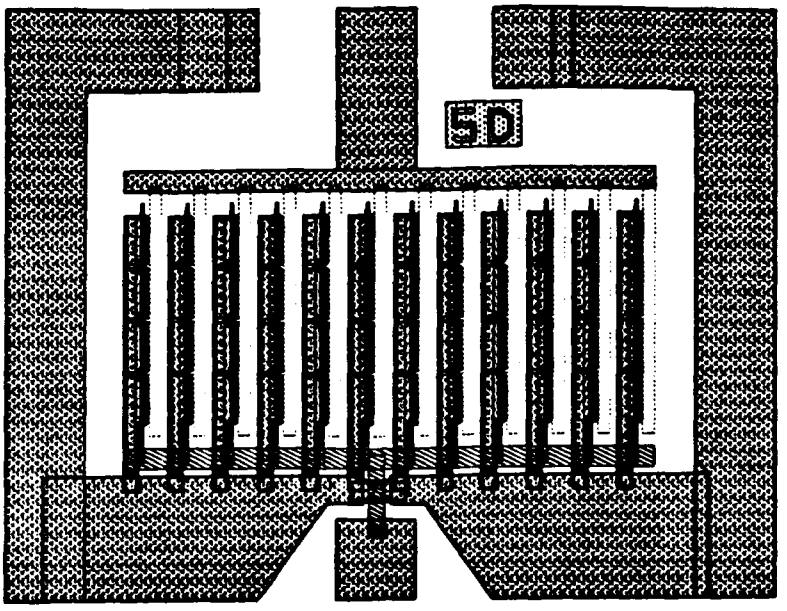

Figure 2-5 Triode 50D divided into 12 cells with four 50 μm wide emitters. This device has a 4 μm long upper and a 3 μm lower electrode.

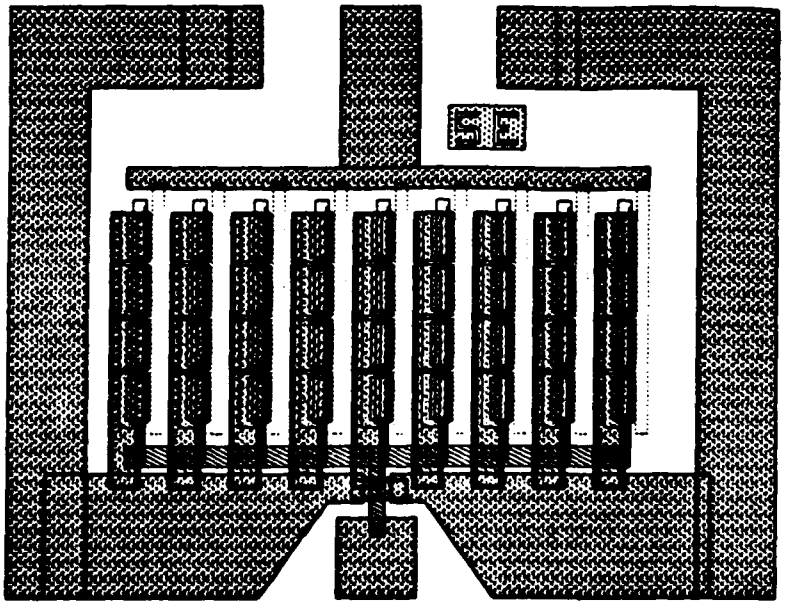

Figure 2-6 Triode 50E divided into 9 cells with four 50 μm wide emitters with resistance in series with each of these emitters.

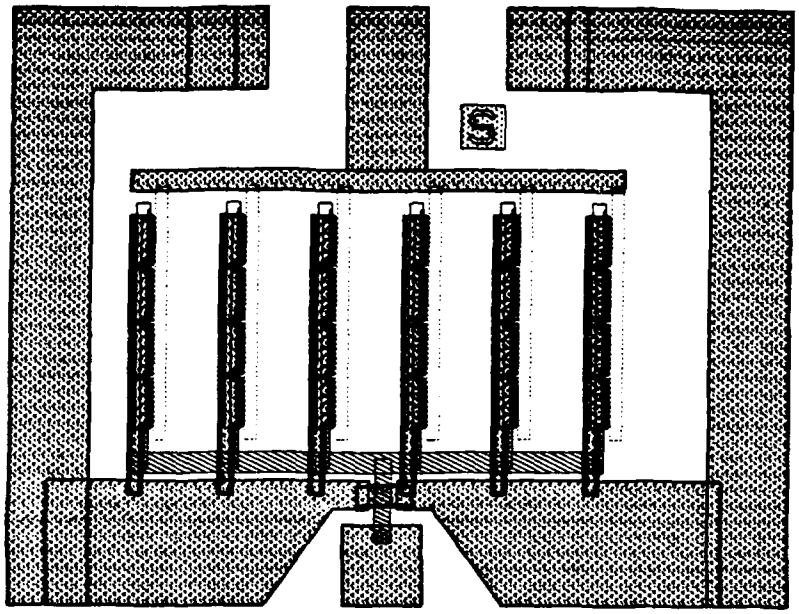

Figure 2-7 Sparse triode divided into six cells with four 50 μm wide emitters to reduce device heating

The fabrication process for these devices is described in Section 3.

3.0 Processing and Mask Layers

The mask layers are given in Table 3-1. To avoid confusion in processing the reticle numbering system is the same as used for mask set 5313 but level 5 has been omitted. The self alignment feature provided in resistor and emitter connection by level 5 is no longer needed with the wafer stepper being used for lithography. Figure 3-1 has the layers used to define one cell of the triode TR-50.

Table 3-1
Mask Level Description

Mask #	Layer #	Description	Polarity
1a	1	Lower control electrode	Light Field
2a	2	Emitter definition	Light Field
3a	3	Emitter contact window for resistor	Dark field
4a	4	Resistor layer	Light Field
6a	6	Emitter and resistor protection cap and emitter edge definition	Light Field
7a	7	Upper sacrificial layer	Light Field
8a	8	Upper control electrode	Light Field
9a	9	Contact window	Dark field
10a	10	Anode and pad metal layer	Light Field

Table 3-2 contains an outline of the process and the various mask levels are listed in Table 3-3.

Table 3-2a
Process Outline

Starting with 3-inch semi-insulating silicon wafers grow 3-4 microns of silicon dioxide:

Layer	Process Description	Parameters	Mask	Polarity
1	**Lower Control Electrode Definition**			
	1000 Å Si_3N_4/1000 Å TiW sputter deposition			
	Control electrode lithography	1811 1.4 µm	001A	LF
	LAM etch TiW/Si_3N_4 in SF_6			
	Resist strip			
2	**Lower Sacrificial Layer Deposition**			
	3500 Å PECVD oxide deposition			
3	**Emitter Definition**			
	500 Å ER Si_3N_4 /1000 Å LS Si_3N_4/300 Å TiW/500 Å BSQ sputter deposition			
	Emitter lithography	1811 1.4 µm	002A	LF
	LAM C_2F_6/CHF_3 BSQ and RIE TiW in SF_6			
	Resist strip			
4	**Emitter Contact Window for Resistor**			
	Lithography	1811 1.4 µm	003A	DF
	Oxide etch in BOE			
	Resist strip			
	1000 Å TaN(or TiW)/200 Å Si_3N_4 sputter deposition			
	Lithography	1811 1.4 µm	004A	LF
	TaN(or TiW) etch in SF_6			
	Resist strip			

Table 3-2b
Process Outline (continued)

Layer	Process Description	Parameters	Mask	Polarity
5	**Emitter and Resistor Protection Cap and Emitter Edge Definition**			
	1000 Å LS + 500 Å ER Si_3N_4 deposition			
	Emitter cap lithography	1805 0.5 µm	006A	LF
	LAM etch of Si_3N_4 in C_2F_6/CHF_3, ion mill TiW, LAM etch Si_3N_4 in C_2F_6/CHF_3			
	Resist strip			
6	**Upper Sacrificial Layer Definition**			
	3500 Å BSQ deposition			
	Lower via lithography	1811 1.4 µm	007A	LF
	Oxide etch in BOE			
	Resist strip			
7	**Upper Control Electrode**			
	2500 Å TiW/2500 Å Si_3N_4 sputter deposition			
	UCE lithography	1818 2.4 µm	008A	LF
	LAM etch Si_3N_4 in C_2F_6/CHF_3			
	LAM etch TiW in SF_6			
	Resist strip			
8	**Anode Window/Via Definition**			
	7500 Å PECVD Oxide Deposition			
	Anode window lithography	1811 1.4 µm	009A	DF
	Oxide etch BOE			
	Resist strip			
9	**Anode Definition**			
	5,000 Å TiW Deposition			
	Anode Lithography	1811 1.4 µm	010A	LF
	LAM or RIE Etch TiW in SF_6			
	Resist strip			

Table 3-2c
Process Outline (continued)

Layer	Process Description	Parameters	Mask	Polarity
10	**In-Process Tests**			
	Line Width and Sheet Resistance Measurements			
	Continuity Measurements			
	Breakdown and Leakage Measurements			
11	**Sacrificial Layer Etch**			
	BOE to obtain a 1 μm lateral etch			
12	**End of Process Tests**			

Table 3-3
Levels Used for Processing the Wafers with the 5366 Mask Set

Level	Field Polarity	Alignment	Critical Dimension
1	LF	Fiducial	4 μm
2	LF	001	4 μm
3	DF	002/001	4 μm
4	LF	002/001	4 μm
6	LF	002/001	4 μm
7	LF	002/001	4 μm
8	LF	002/001	4 μm
9	DF	002/001	4 μm
10	LF	002/001	4 μm